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10/823,030	04/13/2004	Patrick C. Fenton	16437-0209U	3385

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EXAMINER	
NGUYEN, LEON VIET Q	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,030	FENTON, PATRICK C.	
	Examiner	Art Unit	
	Leon-Viet Q. Nguyen	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,21,24-30,32-34,37,38 and 40* is/are rejected.

7)☒ Claim(s) *18-20,22,23,31,35,36 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 10/25/2004 was filed after the mailing date of 10/25/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

1. Claims 9, 19 and 31 are objected to because of the following informalities:

   a. "the array of complex accumulation values" in claims 9, 19, and 31 lack proper antecedent basis.

Appropriate correction is required.

Double Patenting

1. Claims 1-8, 10-17, 21, and 24-30 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 11226174. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Re claim 1, "an array of complex accumulation registers that over multiple code

chips accumulate measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that span all or a portion of a code chip" corresponds to "an array of complex accumulation registers that collect measurements that correspond to samples of the first channel of the received signal over multiple code chips of the first PRN code, the respective accumulation registers being associated with code chip ranges that span all or a portion of a code chip of the first PRN code and all or a portion of a code chip of the second PRN code" and "a code phase decoder that controls the respective complex accumulation registers to direct respective measurements to the complex accumulation registers that are associated with the code chip ranges from which the samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the sample" corresponds to "one or more code phase decoders that control the respective complex accumulation registers to direct respective measurements of the first signal channel of the received signal to the complex accumulation registers that are associated with the respective PRN code chip ranges from which the samples are taken, the one or more code phase decoders decoding values that correspond to the respective estimated phase angles of the samples in the first PRN code to accumulate measurements that relate to chip transitions in the first PRN code and measurements that relate to chip transitions in the second PRN code" in claim 1 of copending Application No. 11226174.

Re claim 2, "the code chip ranges covering a rising edge of the code chip are smaller than the code chip ranges covering other sections of the code chip"

corresponds to "the code chip ranges covering rising code chip edges of one or both of the PRN codes are smaller than the code chip ranges covering other sections of the respective PRN code chips" in claim 7 of copending Application No. 11226174.

Re claim 3, "the code chip ranges are adjustable" corresponds to "the code chip ranges are adjustable" in claim 8 of copending Application No. 11226174.

Re claim 4, "the sizes, numbers and starting points of the code chip ranges are selectively varied" corresponds to "the sizes, numbers and starting points of the code chip ranges associated with one or both PRN codes are selectively varied" in claim 9 of copending Application No. 11226174.

Re claim 5, "the code chip ranges that include an estimated location of the chip edges in a direct path signal are narrowed" corresponds to "the code chip ranges that include an estimated location of the chip edges of the first PRN code in a direct path signal are narrowed for the first PRN code" in claim 10 of copending Application No. 11226174.

Re claim 6, "the starting points of one or more code chip ranges are changed to selectively position the code chip ranges relative to the estimated location of chip edges in a direct path signal" corresponds to "the starting points of one or more code chip ranges are changed to selectively position the code chip ranges relative to the

estimated location of the chip edges of the respective codes in a direct path signal" in claim 11 of copending Application No. 11226174.

Re claim 7, "the number of code chip ranges is reduced after an estimate of the location of chip edges in a direct path signal is calculated" corresponds to "the number of code chip ranges for one or both PRN codes is reduced after an estimate of the location of chip edges in a direct path signal is calculated" " in claim 12 of copending Application No. 11226174.

Re claim 8, "the respective complex accumulation registers include inphase registers that collect measurements that correspond to inphase samples and quadrature phase registers that collect measurements that correspond to quadrature samples" corresponds to "the respective complex accumulation registers include I registers that collect measurements that correspond to in-phase samples and Q phase registers that collect measurements that correspond to quadrature samples" in claim 13 of copending Application No. 11226174.

Re claim 10, "a local code generator that produces phase-delayed versions of a code that is included in the received signal" corresponds to "a local code generator that produces a phase-delayed version of a first PRN code that is included in the first channel of the received signal"; "a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase"

corresponds to "a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase of the first PRN code"; "a carrier phase generator that produces phase angles that correspond to an estimated carrier phase" corresponds to "a carrier phase generator that produces phase angles that correspond to an estimated carrier phase of the first signal channel of the received signal"; "an array of complex accumulation registers that collect measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that span all or a portion of a code chip" corresponds to "an array of complex accumulation registers that collect measurements that correspond to samples of the first channel of the received signal over multiple code chips of the first PRN code, the respective accumulation registers being associated with code chip ranges that span all or a portion of a code chip of the first PRN code"; and "a code phase decoder that controls the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the samples" corresponds to "one or more code phase decoders that control the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the one or more code phase decoders decoding values that correspond to the estimated phase angles of the samples in the first PRN code and providing ranges that relate to chip transitions in the first PRN code and to chip

transitions in the second PRN code" in claim 14 of copending Application No. 11226174.

"A multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals" corresponds to "a multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals" and "adders that combine the code multipath error signals and carrier multipath error signals with the code error signals and phase errors signals, respectively, to correct for code and carrier tracking errors associated with multipath interference, the adders producing the signals that are used to control the code generator and the phase generator" corresponds to "adders that combine the code multipath error signals and carrier multipath error signals with the code error signals and phase errors signals, respectively, to correct for code and carrier tracking errors associated with multipath interference, the adders producing the signals that are used to control the code generator and the phase generator" in claim 15 of copending Application No. 11226174.

"A plurality of multipliers that multiply the respective versions of the code by samples taken of the received signal and produce corresponding measurements" corresponds to "a plurality of multipliers that multiply the respective versions of the code by samples taken of the first channel of the received signal and produce corresponding measurements"; "a code tracking delay lock loop that produces code error signals that are used to control the code rate of the code generator" corresponds to "a code tracking

delay lock loop that produces code error signals that are used to control the code rate of the code generator" ; and "a carrier tracking phase lock loop that produces phase error signals that are used to control the phase generator" corresponds to "a carrier tracking phase lock loop that produces phase error signals that are used to control the phase generator" in claim 16 of copending Application No. 11226174.

Re claim 11, the limitations have been addressed with respect to claim 2 in the current application.

Re claim 12, the limitations have been addressed with respect to claim 3 in the current application.

Re claim 13, the limitations have been addressed with respect to claim 4 in the current application.

Re claim 14, the limitations have been addressed with respect to claim 5 in the current application.

Re claim 15, the limitations have been addressed with respect to claim 6 in the current application.

Re claim 16, the limitations have been addressed with respect to claim 7 in the current application.

Re claim 17, the limitations have been addressed with respect to claim 8 in the current application.

Re claim 21, "a local code generator that produces a phase-delayed version of a code that is included in the received signal" corresponds to "a local code generator that produces a phase-delayed version of a first PRN code that is included in the first channel of the received signal"; "a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase" corresponds to "a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase of the first PRN code"; "a multiplier that multiplies the version of the code by samples taken of the received signal and produces corresponding measurements" corresponds to "a multiplier that multiplies the version of the code by samples taken of the first channel of the received signal and produces corresponding measurements"; "a carrier phase generator that produces phase angles that correspond to an estimated carrier phase" corresponds to "a carrier phase generator that produces phase angles that correspond to an estimated carrier phase of the first signal channel of the received signal"; "an array of complex accumulation registers that collect measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that

span all or a portion of a code chip" corresponds to "an array of complex accumulation registers that collect measurements that correspond to samples of the first channel of the received signal over multiple code chips of the first PRN code, the respective accumulation registers being associated with code chip ranges that span all or a portion of a code chip of the first PRN code"; and "a code phase decoder that controls the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the samples" corresponds to "one or more code phase decoders that control the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the one or more code phase decoders decoding values that correspond to the estimated phase angles of the samples in the first PRN code and providing ranges that relate to chip transitions in the first PRN code and to chip transitions in the second PRN code" in claim 14 of copending Application No. 11226174.

"A multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals" corresponds to "a multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals" in claim 15 of copending Application No. 11226174.

Re claim 24, the limitations have been addressed with respect to claim 2 in the current application.

Re claim 25, the limitations have been addressed with respect to claim 3 in the current application.

Re claim 26, the limitations have been addressed with respect to claim 4 in the current application.

Re claim 27, the limitations have been addressed with respect to claim 5 in the current application.

Re claim 28, the limitations have been addressed with respect to claim 6 in the current application.

Re claim 29, the limitations have been addressed with respect to claim 7 in the current application.

Re claim 30, the limitations have been addressed with respect to claim 8 in the current application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Lorenz et al (US5134407).

Re claim 1, Lorenz discloses a pre-correlation filter for a receiver that receives spread-spectrum signals, the filter including:

an array of complex accumulation registers (accumulators 151 and 155 in fig. 4) that over multiple code chips accumulate measurements that correspond to samples of the received signal (col. 9 line 63 – col. 10 line 4, L1 and L2 are interpreted to be the received signals), the accumulation registers being associated with code chip ranges that span all or a portion of a code chip (col. 9 line 63 – col. 10 line 4, the A-code is interpreted to be the code chip range);

a code phase decoder (carrier generators 107 and 109 in fig. 4) that controls the respective complex accumulation registers to direct respective measurements to the complex accumulation registers that are associated with the code chip ranges from

which the samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the sample (col. 9 lines 7-22 and col. 13 lines 22-34, the replica of the L1 and L2 signals are interpreted to be estimates of the signals).

3. Claims 32 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Underbrink et al (US20050025222).

Re claim 32, Underbrink discloses a method of producing measurement pulse shapes associated with code chips of a PRN code in a received signal, the method including the steps of:

over multiple PRN code chips (¶0013, "one of the PN code chips" it is interpreted to mean that there is more than one code chip) taking measurements that correspond to samples of the received signal (¶0013, the selected portion of the signal sample is interpreted to be a measurement corresponding to that sample); and

selectively combining the measurements into ranges that span all or a portion of a code chip (¶0013, the adder adding the first and second product which corresponds to the measurements from the first and second signal samples), the ranges being based on estimated phase angles of the samples (¶0014. Underbrink discloses that each pair of signal samples has an in-phase and quadrature-phase portion, which is well known to have a phase angle. Therefore it is interpreted that the range is based on the phase angles).

Re claim 37, Underbrink discloses a method wherein the step of taking measurements includes taking measurements that correspond to inphase samples and quadrature samples (¶0013 - ¶0014, the selected portion of the signal sample is interpreted to the measurements and each signal sample includes an in-phase and quadrature-phase portions).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorenz et al (US5134407) and further in view of Stansell, Jr. (US5963582).

Re claim 2, Lorenz fails to teach a pre-correlation filter wherein the code chip ranges covering a rising edge of the code chip are smaller than the code chip ranges covering other sections of the code chip. However Stansell, Jr. teaches the leading edge of a code chip being smaller than other sections of the code chip (fig. 36G, col. 43 lines 15-17).

Therefore taking the combined teachings of Lorenz and Stansell, Jr. as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the smaller leading edge of a code chip of Stansell, Jr. into the

pre-correlation filter of Lorenz. The motivation to combine Stansell, Jr. and Lorenz would be to simplify the logic (col. 43 lines 18-19).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorenz et al (US5134407) and further in view of Zhengdi (US6751247).

Re claim 3, Lorenz fails to teach a pre-correlation filter wherein the code chip ranges are adjustable. However Zhengdi teaches changing a code chip frequency, interpreted to be the code chip range, according to the duration in time of the spreading code and according to the chip length (col. 4 lines 29-33).

Therefore taking the combined teachings of Lorenz and Zhengdi as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the adjustable code chip frequency of Zhegdi into the pre-correlation filter of Lorenz. The motivation to combine Zhengdi and Lorenz would be to reduce correlation between the spreading codes (col. 4 lines 33-34) and detect the signal better (col. 4 line 41).

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorenz et al (US5134407) and further in view of Harms et al (US6493376).

Re claim 4, Lorenz fails to teach a pre-correlation filter wherein the sizes, numbers and starting points of the code chip ranges are selectively varied. However, in ¶0049 of applicant's specification, varying of the length, number, and/or starting position

of the ranges is achieved by changing the code offset values associated with the accumulators.

Harms teaches an accumulator which generates the correlation of the data at each possible local PN code offset time (col. 24 lines 2-5). Although not explicitly stated, one of ordinary skill in the art would have found it obvious and necessary to change the code offset values corresponding to the code offset times.

Therefore taking the combined teachings of Lorenz and Harms as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the changing of code offset values of Harms into the pre-correlation filter of Lorenz. The motivation to combine Harms and Lorenz would be to differentially detect phase shifts between consecutive accumulated signals (col. 6 lines 8-12).

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lorenz et al (US5134407) and further in view of Fenton et al (US5390207).

Re claim 8, Lorenz fails to teach a pre-correlation filter wherein the respective complex accumulation registers include inphase registers that collect measurements that correspond to inphase samples and quadrature phase registers that collect measurements that correspond to quadrature samples. However, Fenton teaches wherein the respective complex accumulation registers include inphase registers (register 244i in fig. 6) that collect measurements that correspond to inphase samples and quadrature phase registers (register 244q in fig. 6) that collect measurements that correspond to quadrature samples.

Therefore taking the combined teachings of Lorenz and Fenton as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the inphase and quadrature registers of Fenton into the pre-correlation filter of Lorenz. The motivation to combine Fenton and Lorenz would be to perform low frequency filtering (col. 10 lines 56-57), which is well known in the art to reduce noise.

Re claim 9, Lorenz fails to teach a pre-correlation filter wherein the array of complex accumulation values are compared with a predetermined reference shape to detect the presence or absence of interfering signals. However Fenton teaches wherein the array of complex accumulation values (col. 10 lines 56-57, the I_D and Q_D data) are compared with a predetermined reference shape (col. 10 lines 56-57, the low frequency filtering function is interpreted to be the reference shape).

Therefore taking the combined teachings of Lorenz and Fenton as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the comparison method of Fenton into the pre-correlation filter of Lorenz. The motivation to combine Fenton and Lorenz would be to perform low frequency filtering (col. 10 lines 56-57), which is well known in the art to reduce noise.

9. Claims 33 and 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Underbrink et al (US20050025222) and further in view of Sanderford et al (US5764686).

Re claim 33, Underbrink fails to teach a method further including the step of determining an estimated location of the chip edges in a direct path signal. However Sanderford teaches correlation peak information which comes from a portion of a chip time or a whole chip time (col. 4 lines 48-52) to estimate a leading edge of the correlation function (col. 4 lines 50-52). The correlation function is interpreted to be the direct path signal.

Therefore taking the combined teachings of Underbrink and Sanderford as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the edge determining method of Sanderford into the method of Underbrink. The motivation to combine Underbrink and Sanderford would be to shorten the dwell time required when taking additional samples of the leading edge of a correlation function (col. 5 lines 35-39).

Re claim 34, the modified invention of Underbrink teaches a method further including the step of narrowing the ranges that are associated with the chip edges (col. 1 lines 43-46, the chip time is interpreted to be the chip range).

10. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Underbrink et al (US20050025222) and further in view of Kohli et al (US6466612).

Re claim 38, Underbrink fails to teach a method wherein the step of combining further includes combining the measurements to produce one or more early correlation values and one or more late correlation values for use in correlating a local PRN code to

the received PRN code and a local carrier to a received carrier. However Kohli teaches combining the measurements to produce one or more early correlation values and one or more late correlation values (col. 17 lines 25-28) for use in correlating a local PRN code to the received PRN code and a local carrier to a received carrier (col. 1 line 66 – col. 2 line 17).

Therefore taking the combined teachings of Underbrink and Kohli as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the production and use of early and late correlation values of Kohli into the method of Underbrink. The motivation to combine Underbrink and Kohli would be to accurately maintain the synchronization of prompt correlation (col. 2 lines 15-17).

11. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Underbrink et al (US20050025222) and further in view of Fenton et al (US5390207).

Re claim 40, Underbrink fails to teach a method further including the step of comparing the combined measurements with a predetermined reference shape to detect the presence or absence of interfering signals. However Fenton teaches comparing the combined measurements (col. 10 lines 43-48, the I_D and Q_D data coming from the addition of two measurements as seen in the equations) with a predetermined reference shape (col. 10 lines 56-57, the low frequency filtering function is interpreted to be the reference shape).

Therefore taking the combined teachings of Underbrink and Fenton as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to incorporate the comparison method of Fenton into the method of Underbrink. The motivation to combine Fenton and Underbrink would be to perform low frequency filtering (col. 10 lines 56-57), which is well known in the art to reduce noise.

Allowable Subject Matter

12. Claims 18-20, 22, 23, 31, 35, 36, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER